## REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on April 5, 2006, and the references cited therewith.

Claims 10 and 14 are amended, as a result, claims 1-21 remain pending in this application.

*Section 103 Rejection of the Claims*

Claims 1-6 were rejected under 35 USC Section 103(a) as allegedly being unpatentable over *Whitt* (U.S. Patent 4,881,243) in view of *Schuur* (U.S. Patent 5,590,157) further in view of *Pasqualini* (U.S. Patent 6,397,374) and further in view of *Gailhard, et al.* (U.S. Patent 6,703,880).

Claims 7-19, 11-12 were rejected under 35 USC Section 103(a) as allegedly being unpatentable over *Whitt* (U.S. Patent 4,881,243) in view of *Schuur* (U.S. Patent 5,590,157) further in view of *Pasqualini* (u.s. Patent 6,397,374) and further in view of *Gailhard, et al.* (U.S. Patent 6,703,880) and in futher view of *Ten Pierick* (U.S. Patent 6,226,344).

Claims 15 and 16 were rejected under 35 USC Section 103(a) as allegedly being unpatentable over *Whitt* in view of *Gailhard, et al.* (U.S. Patent 6,703,880) in futher view of *Ten Pierick* (U.S. Patent 6,226,344) and in futher view of of *Peragine* (U.S. Patent 6,623,185).

Claims 17 and 21 were rejected under 35 USC Section 103(a) as allegedly being unpatentable over *Whitt* (U.S. Patent 4,881,243) in view of *Schuur* (U.S. Patent 5,590,157) further in view of *Pasqualini* (U.S. Patent 6,397,374) and further in view of *Gailhard, et al.* (U.S. Patent 6,703,880) and further in view of *Peragine* (U.S. Patent 6,623,185).

Claims 18 and 19 were rejected under 35 USC Section 103(a) as allegedly being unpatentable over *Whitt* (U.S. Patent 4,881,243) in view of *Schuur* (U.S. Patent 5,590,157) further in view of *Pasqualini* (u.s. Patent 6,397,374) and further in view of *Gailhard, et al.* (U.S. Patent 6,703,880), further in view of *Peragine* (U.S. Patent 6,623,185) and further in view of *Ten Pierick* (U.S. Patent 6,226,344).

Claim 20 was rejected under 35 USC Section 103(a) as allegedly being unpatentable over *Whitt* (U.S. Patent 4,881,243) in view of *Schuur* (U.S. Patent 5,590,157) further in view of *Pasqualini* (U.S. Patent 6,397,374) and further in view of *Gailhard, et al.* (U.S. Patent 6,703,880).

Claim 1 requires a "delay circuit [that] is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal." Claims 2, 4, and 20 also require a symmetrical delay between the clock and data signals. As explained in the specification, the delay circuit is configured to delay the incoming data signal in this manner so that a single flip-flop can be used in the circuit to detect bit errors. When the

extracted CLK signal is loaded down by only a single flip-flop like this, the capacitive load on the high-speed signal path is minimized, such that the claimed loss-of-signal detector can be used with high speed communications standards (e.g., SONET, ATM), e.g., at speeds greater than 10 Gb/s, even when CMOS devices are used. See Application at paragraphs 21, 18, and 17.

The Office action does not cite any reference as disclosing the claimed "delay circuit [that] is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal," but asserts "it is well known in the art to symmetrically delay the incoming data and it would be obvious to one skilled in the art to perform such a task to avoid error before and after the sampled edge." Office action at page 3.

Respectfully, the Office fails to establish a prima facie case of obviousness because the Office fails to provide a motivation to include a symmetric delay with the other elements of the claim. Without agreeing with the statements in the Office action, even if a symmetric delay would "avoid error before and after the sampled edge," this still provides no motivation to combine this feature with other elements of the claim, since there are plenty of other ways of avoiding error before and after a sampled edge. Just because it is possible to combine features from different references does not mean that a motivation to do so exists. As explained above, the symmetric delay is used so that only a single flip-flop is needed in the claimed loss-of-signal circuit, and by using only a single flip-flop capacitive loading on the signal line is reduced, which allows the circuit to be implemented in CMOS devices and used in high-speed applications. Moreover, the object of the claimed circuit is to detect errors in the timing between the extracted clock signal and the data signal, rather than to "avoid errors" as cited in the Office action.

Therefore, because claims 1, 2, 4, and 20 would not have been obvious, applicant respectfully requests allowance of these claims and their base claims.

Claim 15 requires a "SLOS detector [that] is configured such that it adds as capacitive loading a single flip-flop to the recovered clock signal and a single delay circuit to the incoming data signal." The Office action does not allege that this element is found explicitly or implicitly in the prior art, and therefore a prima facie case of obviousness has not been established.

For at least this reason, applicant requests allowance of claim 15 and its dependent claim, claim 16.

*Allowable Subject Matter*

Claims 10 and 14 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 10 and 14 have been rewritten to incorporate the subject matter of their base and intervening claims. Therefore, allowance of claims 10 and 14 is now requested.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. A petition for a two-month extension of time and authorization for a credit card charge of $450 to cover the cost of the petition is enclosed. No other fees are believed to be due at this time. However, if necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521, referencing attorney docket number 0003-081001.

The Examiner is invited to telephone Applicant's attorney (202-787-3833) to facilitate prosecution of this application.

Respectfully submitted,
Brake Hughes PLC
**Customer Number 57246**
202-787-3833

Date September 5, 2006

By _____
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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5th day of September, 2006.

Shellie Bailey

Signature